**Practical-2**

**Aim:**

To verify the truth table of Ex­OR &amp; Ex­NOR gates by

AOI logic.

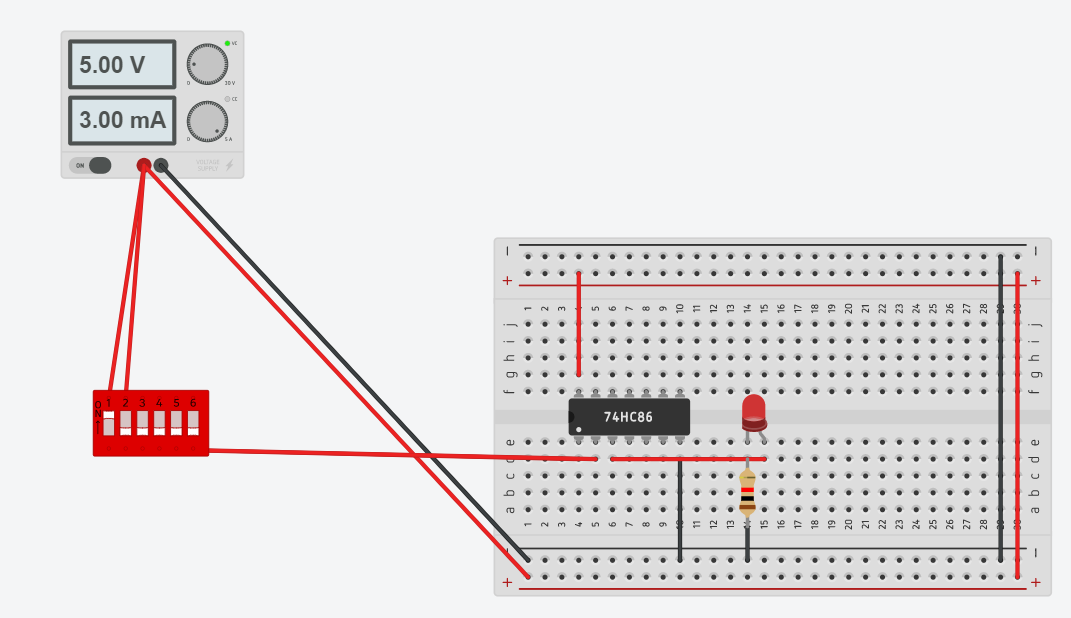
**Apparatus:**

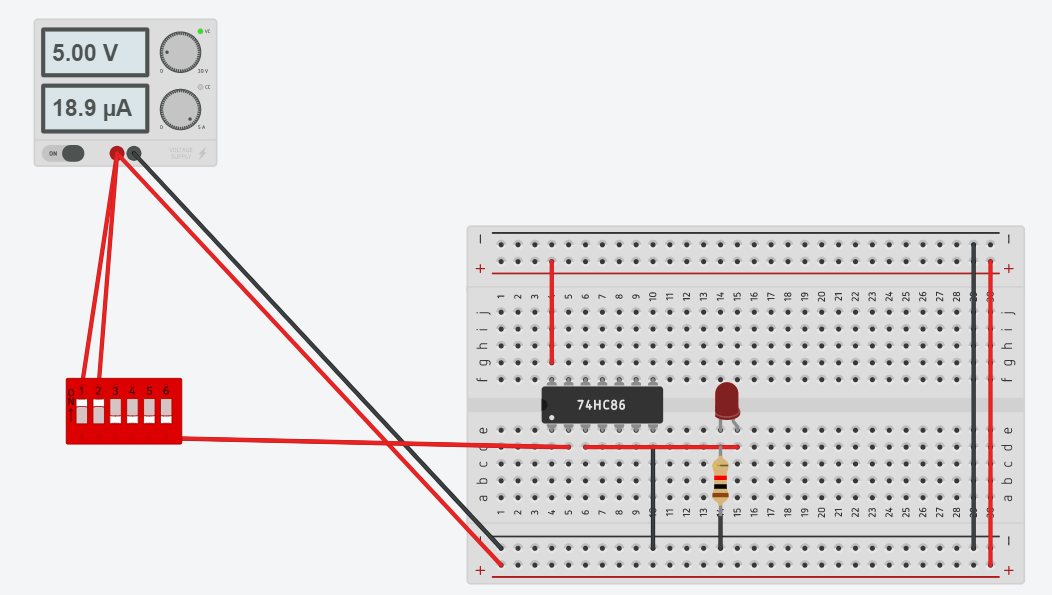
connection wires, power supply, power project board, LED, ICs

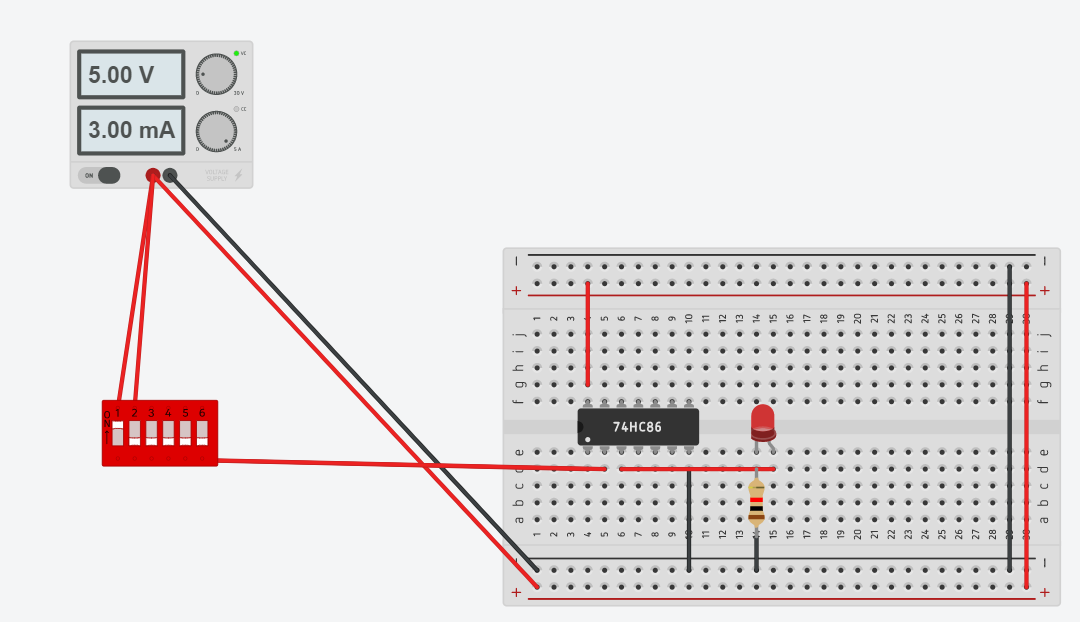
**Theory:**

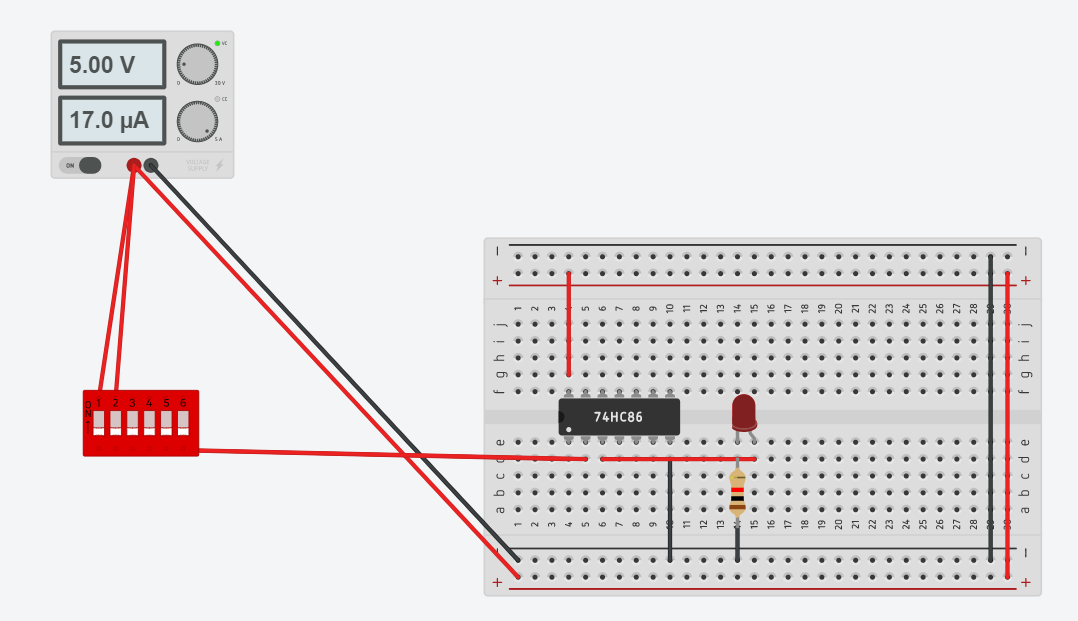
The Ex­OR gate is a two input, one output logic circuit whose output assumes a logic 1 state when one and only one of its two inputs assumes a logic 1 state. Under the conditions when both the inputs assumes the logic 0 state, or when both the inputs assume the logic 1state, the output assumes a logic 0 state. Since an Ex­OR gate produces an output 1 only when the inputs are not equal, it is called an anti­coincidence gate or inequality detector.

2 **Input XOR gate using AOI logic:**









**Observation Table:**

|  |  |  |
| --- | --- | --- |
| INPUT | INPUT | OUTPUT |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The Ex­NOR gate is a two input, one output logic circuit whose output assumes a logic

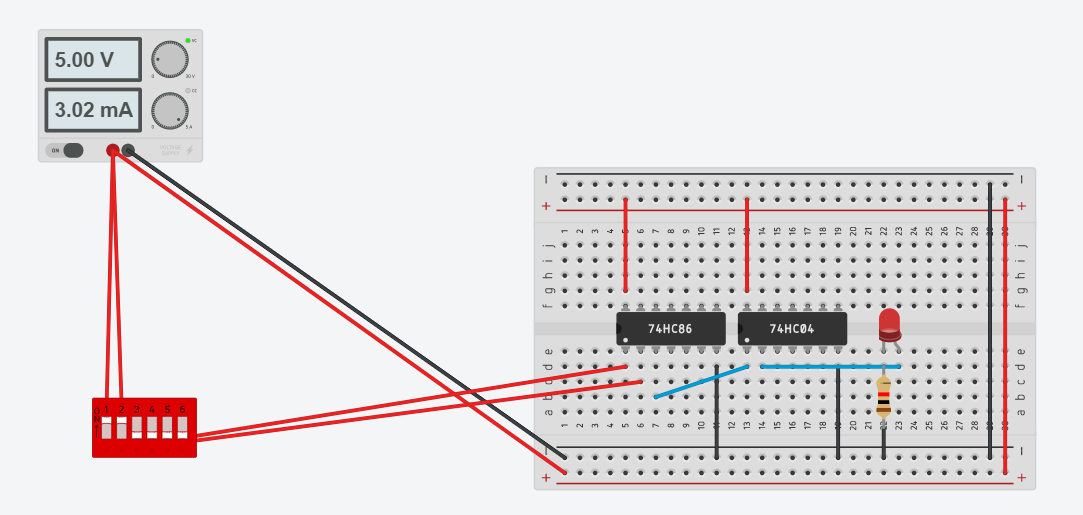
0 state or when both the inputs assumes a logic 1 state. The output assumes a logic 0

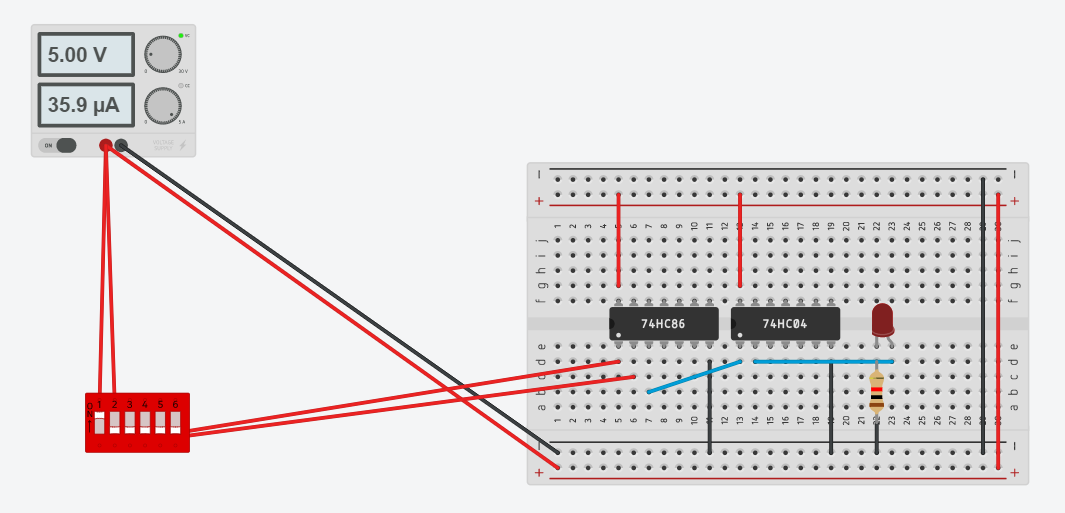
state, when one of the inputs assumes a 0 state and the other a 1 state. It is also

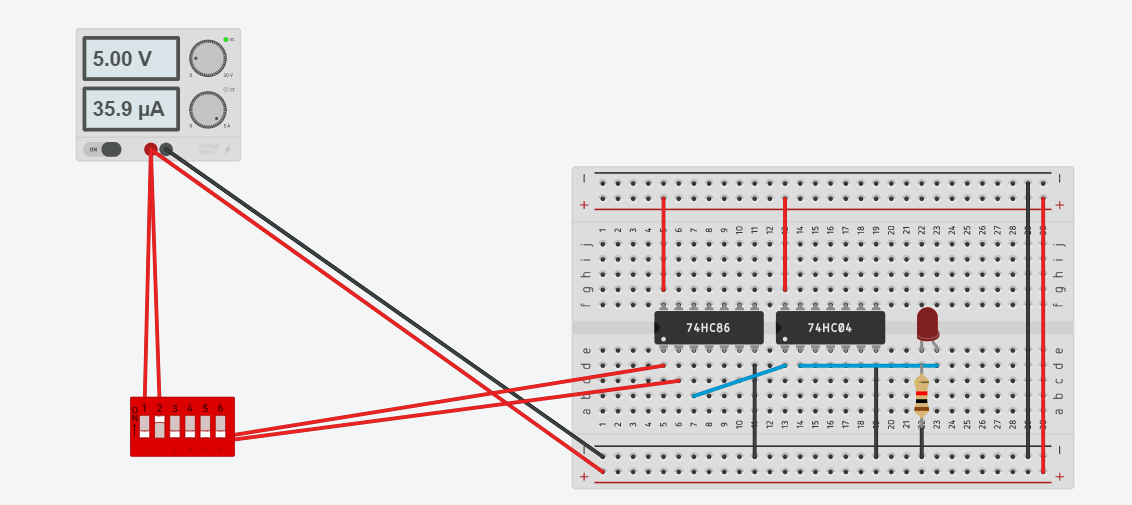
known as a coincidence gate or equality detector.

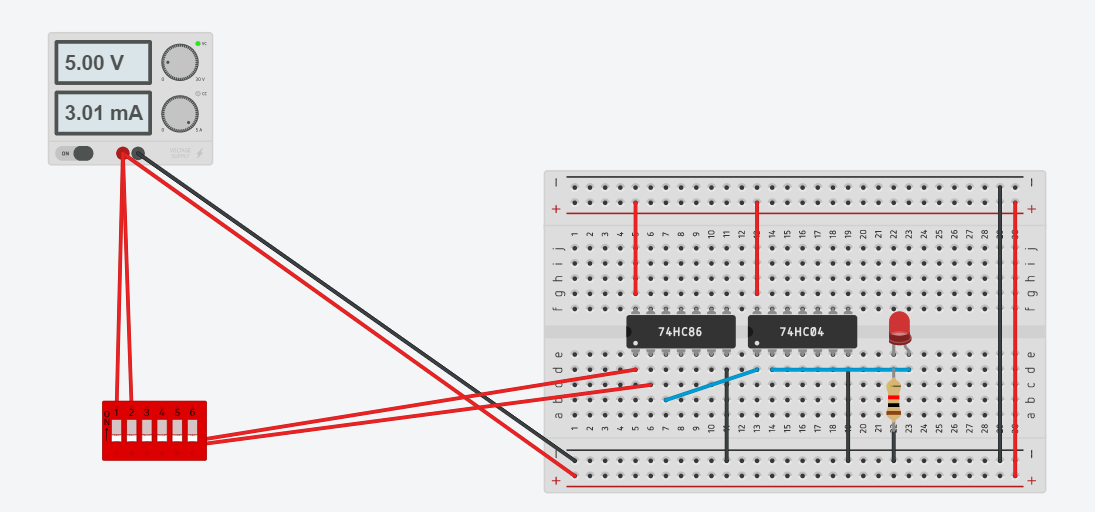


**2 Input Ex­NOR gate using AOI logic:**









**Observation Table:**

|  |  |  |
| --- | --- | --- |
| INPUT | INPUT | OUTPUT |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Procedure:**

1) Connect the circuit according to circuit diagram.

2) Apply different input combination at the input pin of ICs.

3) Verify the truth table of Ex­OR and Ex­NOR gate for different input combinations.

**CONCLUSION:**By performing the above practical, we verified the working of ex-OR and ex-NOR